I claim:

1. An electronic circuit comprising;

A. combinational circuitry to be tested, the combinational circuitry having stimulus inputs and response outputs;

B. a plurality of serial scan paths, each having a serial scan input and a serial scan output, and each connected to communicate test data to separate portions of the combinational circuitry by connection to the stimulus inputs and response outputs;

C. a scan path control circuit having a plurality of separate control output leads, each separate control output lead being connected to one of the plurality of scan paths, the scan path control circuit outputs control to the plurality of scan paths, such that only one scan path is active at a time to input and output test data from the scan inputs and scan outputs.

2. The circuit of claim 1 in which the control circuit is a state machine.

3. The circuit of claim 1 in which the control circuit is a sate machine having an Idle state, a Capture state and a Shift state for each scan path.

4. The circuit of claim 1 in which the serial scan inputs of all the scan paths are connected to one another and the serial scan outputs of all the scan paths are connected to one another.

5. The circuit of claim 1 in which the serial scan inputs are separate from one another and the serial scan outputs are separate from one another and the scan paths are in parallel with one another.

6. A process of testing combinational logic having response outputs connected to plural scan paths, comprising:

A. performing a capture operation by loading data from the response outputs into the scan paths;

B. performing a shift operation on a first scan path without performing a shift operation on any other scan path; and

C. performing a shift operation on a second scan path without performing a shift operation on any other scan path.